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TITLE	**Table of Content for Quantum Computing Hardware**
PROJECT	FGQT Roadmap
REFERRING TO	"N020 Contribution on ToC"
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This update N058a is mainly a layout revision of N058, in order to achieve a clear separation between "editorial notes" and proposed text.

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ABSTRACT

Explanation of changes

We propose a way forward to describe more dedicated needs and requirements on some of the modules needed within Quantum Computing. The proposal is to break this challenge down into smaller pieces. Our proposal elaborates mainly on low level hardware implementations of solid-state quantum computing architectures. We leave other hardware implementations (such as trapped-ion based solutions and other/future architectures) as well as higher software layers to proposals from other delegates.

Why are the changes needed?

We need a way forward, to get progress on at least some of the implementations of Quantum Computers. Since some QC hardware implementations are more mature than others, it makes sense to break the problem down along these lines so that we get progress on those that are more mature.

1. Situation sketch

Quantum computing is an area covering very different implementations and each implementation has its own dedicated solution and maturity. The aim is a stack of soft and hardware layers, where higher layers are more agnostic for these differences than lower layers.
At the bottom (hardware side) of this stack, solutions are to be very dedicated to these differences. Figure 1 may be illustrative for that part of the stack.
We have elaborated more on solid-state quantum architectures, but optical and other hardware solutions deserve a similar elaboration on their details. We leave that to other experts. The same applies for the software layers higher-up in the stack.

We propose to fill section 4.3 of the roadmap document only with generic/functional (less detailed) descriptions on the various concepts of quantum computing, and to describe further details in *different* annexes on (a) solid-state quantum architectures, (b) optical quantum solutions, (c) other quantum implementations, and (d) software layers.

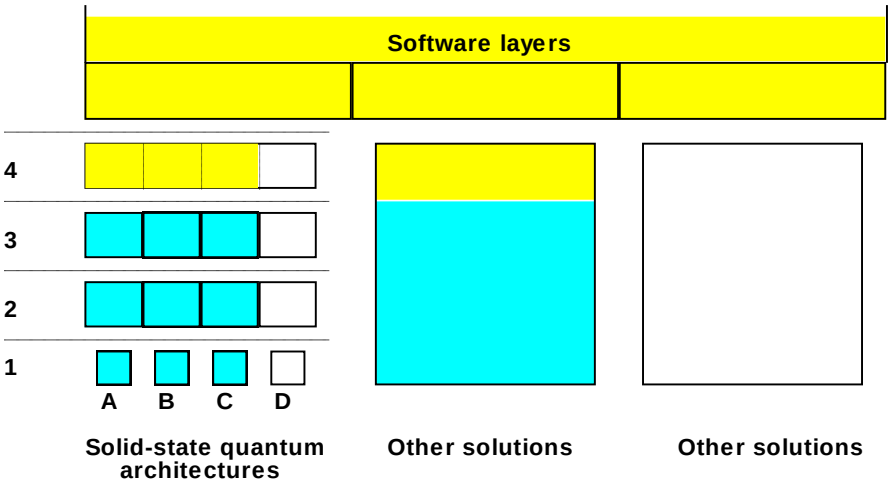
Proposal for inclusion in section 4.3

4.3.4 Modularity and layering of hardware stack

Quantum computing is an area covering very different architectures and each architecture has its own dedicated implementation. A convenient way of describing them is by using a layered stack, ranging from hardware at the bottom to software at the top.
When needed, each layer can be subdivided into different modules that are dedicated to a specific architecture. Figure 1 illustrates a possible layering and modularity, for the purpose of organizing this text..

Editorial note: Figure 1 is currently only dedicated to solid-state quantum architectures. We suggest upgrading this picture as soon as relevant details on other architectures are contributed to FGQT. The first block in figure 1 covers solid-state quantum architecture. The second block could cover optical (trapped-ion) architectures. The third block symbolize the existence of even more architectures.

Editorial note: If the word “architecture” is not the most appropriated terminology, we may replace it by words like “architecture family”, “category”, “implementation group”, “solutions”, “technology”, “principle” or whatsoever. This does not change the intention of the text.



A = Transmons
B = Spin qubits
C = NV Centers
D = Some future development

1 = Quantum Device (Chip, PCB, ..) at Cryogenic temperatures
2 = Quantum Control Highway (interconnect, filtering, amplification..)
3 = Quantum Control Electronics (room temperature electronics, software interface, ..)
4 = Quantum Control Software (drivers, calibration, ...)

Figure 1. A possible break-down of quantum computing architectures into various modules

4.3.4.1 Solid-state based quantum computing architectures

These architectures have in common that they all make use of a cryogenic fridge, where the quantum device is controlled from outside the fridge by room-temperature electronics. Consequently, a huge amount of control channels is required to interconnect those two, especially when many qubits are to be controlled in a single fridge.

Editorial note: This section should at least elaborate on a high-level functional description of different quantum computing architectures, and what cryogenic conditions they require to operate. This should include at least NV centers, Transmon architectures, Spin-qubit architectures, and does not exclude others.
This text is mainly introductory in nature. But the more technical details on requirements and needs are elaborated in a more dedicated annex “X”.

Editorial note: This section should also elaborate on a high-level functional description of the various modules (see figure 1):

- *Quantum Devices*, often being chips on PCB’s. It should also describe a bit on the cryogenic conditions for proper operation.
- *Quantum Control Highway*, being the interconnection between room-temperature electronics and cryogenic devices. It is a mix of transmission lines, filtering, attenuation, amplification, (de)multiplexing, etc. A huge number of control channels are required to control many qubits in a single fridge (which clarifies the name) and this can easily become very bulky. It has also tough requirements on thermal aspects and has filtering and attenuation requirements to reduce noise into quantum devices.
- *Quantum Control Electronics*, being all room-temperature electronics for generating all kinds of pulses (modulated or not) to let a Quantum Device operate. Some implementations make use of routing/switching and/or multiplexing of control signals at room temperatures. If so, this is the place to describe it

- *Quantum Control Software*, being all driver software and other low-level software for instructing the control electronics what signals should be generated or detected, and at what control channel. It also has a software interface to receive instructions about what pulses are to be generated, and how to read-out the response of each.

4.3.4.2 Other solutions #1

Editorial note: This section could be focused on optical architectures like trapped-ion quantum computers. Experts, who are more dedicated to this field, are invited to elaborate on relevant text and naming for this section

4.3.4.3 Other solutions #2

Editorial note: There are more architectures on quantum computing, each with a different state of maturity. Experts, who are more dedicated to those architectures are invited to elaborate on relevant text and naming for this section

4.3.5 Modularity and layering of software stack

Editorial note: It is expected that so many software layers and software modules that their description should cover in multiple subsection
Experts, who are more dedicated to software are invited to elaborate on relevant text and associated naming.

Proposal for creation a dedicated annex „X“

Annex X: Solid-state Quantum Computing

Editorial note: This Roadmap document does not provide any specification since the creation of a standard is out of its scope. However, the identified requirements (without values) may serve as a starting point for future standards. Therefore, this annex is already organized with that purpose in mind.

x.1 Scope and objectives

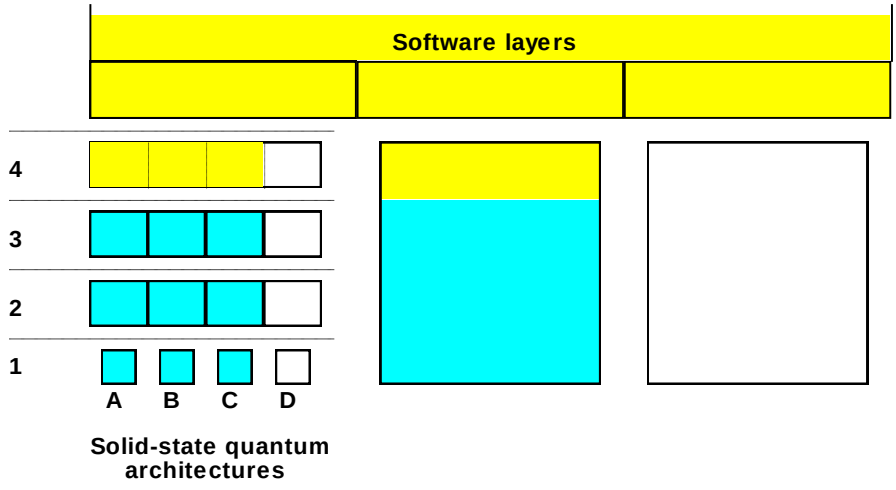


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Figure X.1. A possible break-down into modules for solid-state quantum computing architectures

x.2 Terminology

x.3 References

x.4 Quantum Devices

Editorial note: This section may cover all relevant aspects to let solid-state based quantum devices operate. It may include Transmons, Spin Qubits and NV Centers (and others). Moreover, there are many different Transmon based architectures (differences are 2D, 3D and/or the type of coupling used for connectivity), and many different types of superconducting qubits (fluxonium, flux-qubit, transmons, charge qubit, etc.), which might have different requirements as well.

Editorial note: This section may summarize a variety of requirements that deserve a specification. Note that the specifications (and values) themselves are out of scope. This inventory may include requirements about signal, thermal and shielding (magnetic and radiation) aspects, as well as how they can be interconnected with the Control Highway. When needed some of these requirements are only relevant to some oft he mentioned technologies.

x.5 Control Highway

Editorial note: This section covers all requirements related to interconnect Quantum Devices with room-temperature electronics. It may contain a common part as well as dedicated sections with different needs per technology. Most components of the control highway are passive (to minimize heat production) but active components (like cryogenic amplification) are not excluded.

Editorial note: So far, the following requirements are identified

- Functional description
  - (filtering, attenuation, amplification, …)
  - (noise aspects, in relation to different temperature stages)
- Transmission requirements
  - (loss, bandwidth, crosstalk, …)
- Thermal requirements
  - (max heat flow, thermal clamping, …)
- Vacuum requirements
  - (what leakage is allowed, and how about aging)
- (non) Magnetic requirements and shielding
- Footprint requirements
  - (how to organize thousands of channels for controlling > 1000 qubits in a single fridge and to feed-back their response)
- Connectivity requirements (with both quantum devices and control electronics)

x.6 Quantum Control Electronics

Editorial note: This section covers all room-temperature electronics for generating the desired pulses and to read-out their response.

- The functional description does not only include the blocks for generating and detecting pulses, but also multiplexing and/or routing/switching functionality (when appropriated)
- The identified requirements may include topics such as signal levels, pulse shapes, noise, etc.
- This section may also describe what interfacing is required with the Control Software layer.

x.7 Quantum Control Software

Editorial note: This section covers hardware specific software to control what pulses are to be generated by the quantum control unit(s) and how to interface them with higher software layers.
It may also identify various needs for calibration and benchmarking.